What is Claimed is:

1. A semiconductor body containing a semiconductor structure and comprising:

the semiconductor body defining an isolation trench having sidewalls and upper and lower portions, and encircling an area of the semiconductor body which contains a semiconductor structure which is to be electrically isolated from other semiconductor structures contained within the semiconductor body but not located within the encircled area;

the lower portion of the isolation trench being at least partly filled with an electrically conductive material that has sidewall portions thereof which are at least partly separated from the sidewalls of the lower portion of the trench by a first electrical insulator, and that has a lower portion that is in electrical contact with the semiconductor body; and

the upper portion of the isolation trench being filled with a second electrical insulator.

2. The semiconductor body of claim 1 wherein the electrically conductive material is doped polysilicon and the first and second electrical insulators are both silicon dioxide.

3. A dynamic random access memory comprising:

a plurality of memory cells arranged in rows and columns in active areas of a semiconductor body with the active areas being separated from one another by a continuous isolation trench in the semiconductor body;

the isolation trench having side walls and upper and lower portions;

the lower portion of the isolation trench being filled with an electrically conductive material that has sidewall portions thereof which are at

least partly separated from the sidewalls of the lower portion of the trench by a first electrical insulator, and that has a lower portion thereof that is in electrical contact with the semiconductor body; and

the upper portion of the isolation trench being filled with a second electrical insulator.

4. The dynamic random access memory of claim 3 in which the active areas are formed in the semiconductor body in a monocrystalline surface well of one conductivity type and the doped polysilicon in the lower portion of the isolation trench is of the one conductivity type and makes a conductive connection to the semiconductor body.

5. A dynamic random access memory comprising:

a memory portion comprising a plurality of memory cells arranged in rows and columns in active areas of a semiconductor body with each memory cell comprising a transistor of one conductivity type and a storage capacitor, and with the active areas being electrically isolated from one another by a first isolation trench in the semiconductor body having a lower portion filled with doped polysilicon and an upper portion filled with an electrical insulator;

the lower portion of the doped polysilicon fill makes electrical contact with the semiconductor body, and sidewall portions of the doped polysilicon fill are electrically isolated from portions of sidewalls of the lower portion of the trench by an electrical insulating layer; and

a peripheral portion comprising circuits which at least comprise one transistor of the one conductivity type and one transistor of an opposite conductivity type in the semiconductor body with circuits of the periphery portion being electrically isolated from one another by a second isolation trench in the semiconductor body that is filled with an electrical insulator.

6. The dynamic random access memory of claim 5 wherein pairs of memory cells are isolated from each other by portions of the first isolation trench and the electrical insulator and the electrical insulating layer are both silicon dioxide.

7. The dynamic random access memory of claim 5 wherein the first isolation trench is continuous.

8. A dynamic random access memory comprising:

a semiconductor body in which there is included an array of memory cells spaced apart from one another and arranged in rows and columns in an active surface layer of one conductivity type;

pairs of memory cells are spaced apart in the semiconductor body by a continuous isolation trench in the semiconductor body that includes as fill a top layer portion that is of a dielectric material and a bottom layer portion that is of polysilicon that is doped to be of said one conductivity type and designed to be maintained at a potential that repels carriers of the kind that are in the minority in it; and

a lower portion of the doped polysilicon fill makes electrical contact with the semiconductor body, and side wall portions of the doped polysilicon fill are electrically isolated from portions of sidewalls of the lower portion of the trench by an electrical insulating layer.

9. A dynamic random access memory comprising:

an array of memory cells formed in a well of one conductivity type in a silicon chip and arranged in rows and columns, each memory cell including a transistor and a storage capacitor;

a continuous isolation trench formed in the well for electrically isolating from one another, within the well, pairs of individual memory cells, said

continuous isolation trench having an upper portion that is filled with a dielectric material and a lower portion that is filled with polysilicon doped to be of the conductivity type of the well; and

a lower portion of the doped polysilicon fill makes electrical contact with the well, and sidewall portions of the doped polysilicon fill are electrically isolated from portions of sidewalls of the lower portion of the trench by an electrical insulating layer.

10. The dynamic random access memory of claim 9 memory in which the storage capacitor of each memory cell is formed by a storage trench that is filled with polysilicon that is electrically isolated from the well and is connected electrically to a source of the transistor of the memory cell by a conductive strap, which includes an outdiffused region, and the drains of each of the transistors in a common column are connected together by a common bit line.

11. The dynamic random access memory of claim 10 in which the top of the lower filled portion of the continuous isolation trench is no higher than a bottom portion of the drains of transistors of a row of memory cells and the bottom of the lower filled portion is at least as deep as the bottom of the strap that connects the fill of the storage trench with a source of the transistor.

12. The dynamic random access memory of claim 11 in which the dielectric fill of the continuous isolation trench is of silicon oxide.

13. The dynamic random access memory of claim 9 in which the well is of p-type conductivity, the transistors are n-channel metal-oxide-semiconductor field effect transistors which form p-n junctions with the well, the lower portion of the isolation trench is filled with p-type polysilicon, and the storage trench is filled with n-type polysilicon.

14. The dynamic random access memory of claim 11 in which the bottom level of the dielectric material in the isolation trench is at least as deep as the deepest source-semiconductor and drain-semiconductor p-n junctions in the silicon semiconductor body in which the memory is formed.

15. A dynamic random access memory comprising:

a monocrystalline silicon chip including a plurality of active areas in each of which there is included a pair of transistors and a pair of separate storage trenches for providing a storage capacitor for each of the transistors;

a continuous isolation trench in the silicon chip for isolating from one another the active areas, the storage trenches being filled with doped polysilicon of one conductivity type;

the isolation trenches having an upper portion filled with a dielectric material and a lower portion filled with doped polysilicon of the conductivity opposite said one conductivity type and connected to a portion of the silicon chip; and

a lower portion of the doped polysilicon fill makes electrical contact with the silicon chip, and side wall portions of the doped polysilicon fill are electrically isolated from portions of sidewalls of the lower portion of the trench by an electrical insulating layer.

16. The dynamic random access memory of claim 15 in which each transistor includes a localized region of the one conductivity type that is connected to the doped polysilicon fill of the one conductivity type of its associated storage trench.

17. The common dynamic random access memory of claim 16 in which the silicon chip includes a p-type well at a top surface thereof in which are included all the active areas of the memory cells, the transistors are n-channel

metal-oxide-semiconductor field effect transistors, the storage trenches are filled with n-type doped polysilicon, and the lower portion fill of the continuous isolation trench is p-type doped polysilicon.

18. A method of providing electrical isolation for semiconductor structures contained in a semiconductor body comprising the steps of:

forming an isolation trench in a portion of the semiconductor body which encircles an area of the semiconductor body;

lining sidewalls of a lower portion of the trench with an electrical insulator;

filling the lower portion of the isolation trench with a conductive material having a lower portion that which makes electrical contact with the semiconductor body and having other portions which are electrically isolated from the sidewalls of the lower portion of the isolation trench by the electrical insulator; and

filling an upper portion of the isolation trench with an electrical insulator.

19. The method of claim of claim 18 wherein the conductive material is doped polysilicon and the electrical insulator are both of silicon dioxide.

20. A method for making memory cells in a semiconductor body of one conductivity type comprising the steps of:

providing a patterned PAD layer over a top surface of the semiconductor body that defines active areas in which memory cells are to be formed, and a continuous field shield isolation trench area;

forming storage trenches in the active areas and filling each with doped polysilicon that is of the conductivity type opposite that of the one

conductivity and that is electrically isolated from the monocrystalline silicon except at a strap region;

forming a continuous isolation trench in the isolation trench area;

forming an electrical insulating layer on sidewalls of a lower portion of the isolation trench;

filling a bottom portion of the isolation trench with doped polysilicon that is of the one conductivity type and that is electrically isolated from the semiconductor body except at the bottom of the isolation trench;

filling the upper portion of the isolation trench with silicon oxide;

forming in each active area a pair of metal-oxide-semiconductor field effect transistors having source and drain regions that are spaced apart and that are each of the opposite conductivity type of the one conductivity type; and

providing a conductive connection between the source of each transistor and the polysilicon fill of a storage trench by way of a strap region.